We claim:

1. An integrated circuit metal oxide semiconductor transistor comprising:

an active region including a gate positioned between a source and a drain;

a silicon germanium layer incorporated into the active region; and

a dielectric layer aligned with said gate and positioned between said gate and said silicon germanium layer, wherein said dielectric layer is formed after thermal processing of said transistor such that said dielectric layer is substantially free of germanium diffused therein from said silicon germanium layer.

2. The transistor of claim 1 wherein said dielectric layer includes less than one percent germanium.

3. The transistor of claim 1 wherein said dielectric layer has a thickness in a range of zero to 100nm.

4. The transistor of claim 1 wherein said dielectric layer is manufactured of a material chosen from the group consisting of tantalum oxide (Ta_2O_5), titanium oxide (TiO_2) zirconium oxide (ZrO_2), lanthanum oxide (La_2O_3), hafnium oxide (HfO_2) yttrium oxide (Y_2O_3), and their silicates.

5. The transistor of claim 1 wherein said silicon germanium layer comprises $Si_{1-x}Ge_x$, wherein x is in a range of 0.05 to 1.0, and wherein said silicon germanium layer has a thickness in a range of 2nm to 5μm.

6. The transistor of claim 1 wherein said gate is manufactured of a material chosen from the group consisting of Pt, W, TiN, Cu, Ir, Ti, Zr, Hf, Ta, TaN, WN and Al.

7. The transistor of claim 1 further comprising a silicon cap layer positioned between said silicon germanium layer and said dielectric layer.

8. A device gate replacement process conducted after high temperature treatment of the device so as to minimize diffusion of germanium into the gate dielectric material, comprising the steps of:

providing a substrate;

depositing a silicon germanium layer on said substrate;

depositing a dummy gate on said silicon germanium layer to define a device, wherein said dummy gate is positioned between a source region and a drain region of the substrate;

subjecting the device to high temperature thermal processing;

removing the dummy gate to define a gate region;

depositing a dielectric material and a final gate material in said gate region, wherein said dielectric material is substantially free of germanium diffused therein.

9. The method of claim 8 wherein said step of removing the dummy gate comprises conducting a selective etch including a step chosen from the group consisting of conducting a phosphoric acid etch and conducting a plasma etch.

10. The method of claim 8, prior to the step of depositing said dummy gate, further comprising the steps of depositing a silicon cap layer on said silicon germanium layer, and depositing a dummy oxide layer on said silicon cap layer, wherein said step of depositing said dummy gate comprises depositing said dummy gate on said dummy oxide layer.

11. The method of claim 8, prior to said step of subjecting the device to high temperature thermal processing, further comprising the steps of forming a source in said

source region adjacent said dummy gate, and forming a drain in said drain region adjacent said dummy gate.

12. The method of claim 8, prior to said step of subjecting the device to high temperature thermal processing, further comprising the steps of depositing an oxide layer over said dummy gate and planarizing the device to expose said dummy gate.

13. The method of claim 8 wherein said dummy gate is fabricated from a material chosen from the group consisting of polysilicon, polysilicon germanium and silicon nitride.

14. The method of claim 8 wherein said high temperature thermal processing comprises subjecting said device to a temperature greater than 700 degrees Celsius for a time period greater than one second.

15. A device fabricated by the method of claim 8.

16. A method of producing a high performance integrated circuit comprising the steps of:

providing a substrate including a source region, a drain region, and a gate region positioned there between;

depositing a silicon germanium layer on said substrate in said gate region;

depositing a silicon cap layer on said silicon germanium layer in said gate region;

depositing a dummy oxide layer on said silicon cap layer in said gate region;

depositing a dummy gate on said silicon cap layer to define a device;

subjecting the device to at least one high temperature thermal process, conducted at a temperature greater than 700 degrees Celsius;

removing the dummy gate to define a gate cast in said gate region;

depositing a dielectric material and a final gate material in said gate cast, wherein said dielectric material is substantially free of germanium diffused therein.

17. The method of claim 16 wherein said step of removing the dummy gate comprises etching said dummy gate and said dummy oxide layer in said gate region.

18. The method of claim 16, prior to said step of subjecting the device to at least one high temperature thermal process, further comprising the steps of forming a source in said source region adjacent said dummy gate, forming a drain in said drain region adjacent said dummy gate, depositing an oxide layer over said dummy gate and planarizing the device to expose said dummy gate.

19. The method of claim 16 wherein said step of depositing a dielectric material comprises depositing said dielectric material on a lower surface and on a sidewall of said gate cast, and wherein said step of depositing said final gate material comprises depositing a final gate material on said dielectric material.